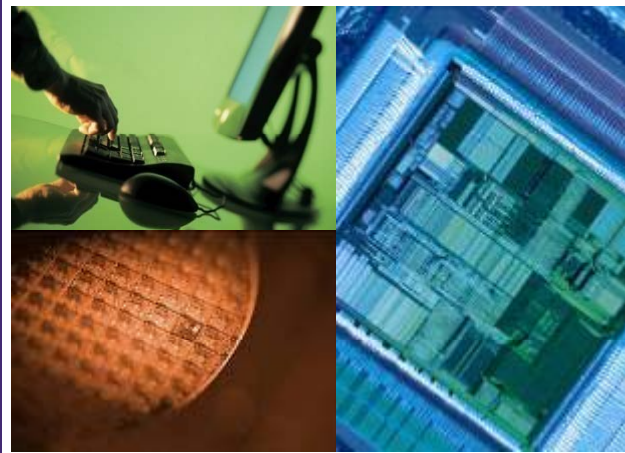


DesignWare Verification IP for OCP



SYNOPSYS[®]
Predictable Success

DesignWare VIP for OCP



SYNOPSYS JOINS OCP-IP GOVERNING STEERING COMMITTEE

BEAVERTON, OR. – October 16, 2007 – Open Core Protocol International Partnership (OCP-IP) today announced that Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, has joined the OCP-IP Governing Steering Committee (GSC). Synopsys' membership augments a highly talented team drawn from members including Nokia, Texas Instruments, Toshiba, and Sonics Inc. Synopsys is active in OCP-IP's working groups, and their DesignWare® Verification IP for OCP interface is a part of the [CoreCreator](#) verification toolset that all OCP-IP community members receive. By joining the GSC, Synopsys, with its extensive SoC design and verification experience, will contribute to OCP-IP's charter to help ensure full play interoperability between on-chip blocks, IP and subsystems.



OCP-IP Unveils CoreCreator II

PORTLAND, ORE – March 04, 2008 – Open Core Protocol International Partnership (OCP-IP) today announced the availability of CoreCreator® II. CoreCreator II features verification IP and command-line based tools for validating Open Core Protocol (OCP) implementations, reducing design time and risk, and enabling rapid time to market.

CoreCreator II allows users to verify, debug, and analyze OCP cores and OCP-based systems. It is comprised of two fundamental component parts: first, Synopsys' [DesignWare® verification IP](#) provides OCP master and slave transactors that generate and respond to all types of OCP 2.2 transactions, and a simulation monitor that provides coverage reports of the functional coverage groups defined in the Protocol Compliance section of the OCP Specification. Second, Sonics' performance analyzer (ocpperf2) and disassembler (ocpdis2) measure interface performance and help view the behavior of OCP traffic. Both component parts are configurable to support the wide range of OCP 2.2 interface options.














OCP-IP STANDARDIZES ON SYNOPSYS' DESIGNWARE VERIFICATION IP FOR OCP-IP'S CORECREATOR VERIFICATION TOOLSET

Collaboration Delivers OCP-compliant Verification Solution for Improved Interoperability and Quality of OCP designs

MOUNTAIN VIEW, Calif. and BEAVERTON, OR – April 10, 2007 - Synopsys, Inc. (Nasdaq:SNPS), a world leader in semiconductor design software, and Open Core Protocol International Partnership (OCP-IP), an independent non-profit semiconductor industry consortium, today announced that they are collaborating to provide Synopsys' DesignWare® Verification IP (VIP) as part of OCP-IP's CoreCreator verification toolset. DesignWare VIP for OCP, part of Synopsys' portfolio of standards-based verification IP, will become the OCP-IP endorsed verification IP solution and will replace the OCP Bus Functional Models (BFM) currently provided with OCP's CoreCreator tool. The new, combined solution, which includes DesignWare VIP and CoreCreator's performance analysis, protocol checking, and transaction disassembly, gives OCP-IP members a common verification toolset, enabling maximum consistency and interoperability across OCP implementations. The collaboration also further expands OCP-IP's robust thriving infrastructure.

DesignWare® Verification IP (VIP) Portfolio

Title		Current Interfaces
AMBA 3 AXI		AXI APB3
AMBA 2.0 AHB, APB		AHB 2.0 APB 2.0
OCP 2.2		OCP 2.0/2.1/2.2
USB		USB 1.1 USB 2.0 USB OTG
PCI Express		PCIe 1.1 PCIe 2.0
Serial ATA 2.5 Device		Gen I 1.5 Gbps Gen II 3.0 Gbps
10/100/1G/10G Ethernet		XGMII
		XAUI
		SGMII
		RGMII
		GMII
		SMII
		MII
PCI		PCI 2.3
		PCI-X 1.0
		PCI-X 2.0
Serial IO		RS232
		GPIO
		IrDa
I2C		I2C
10,000 Memory Models		SRAM SDRAM, DDR II SDRAM, FLASH, etc

- **Common infrastructure / usage style**
 - Simplifies multiple-model usage
 - Easy to learn new titles
- **Used in a wide variety of environments**
 - Easy to integrate into your current methodology
 - Verilog, SystemVerilog and VHDL
 - All popular simulators
 - Directed and Constrained Random Environments
 - Integrated in Synopsys Discovery™ platform
 - Native for higher performance
 - Verification Methodology Manual (VMM)
- **Used at over 600 customer sites**
 - Proven by 1000s of users

DesignWare® Portfolio

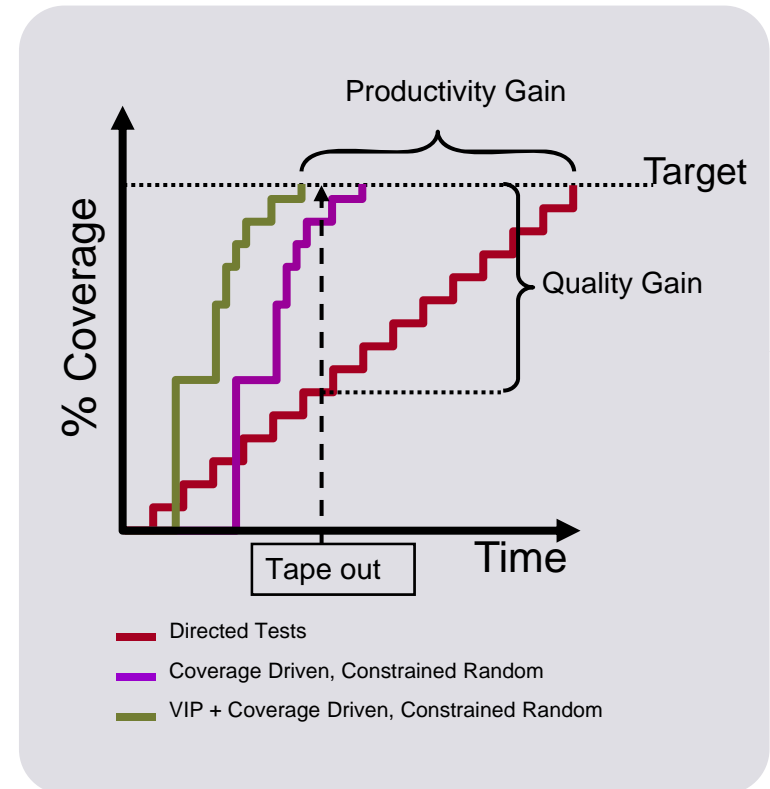
DesignWare Cores	DesignWare Library	VCS Verification Library	DesignWare System-Level Library
<ul style="list-style-type: none"> ■ PCI Express™ ■ PCI Express PHY ■ USB 2.0 OTG... ■ USB 2.0 PHY ■ SATA ■ Ethernet ■ DDR3/DDR2/DDR ■ Wireless USB ■ More.... 	<ul style="list-style-type: none"> ■ Datapath ■ Memory ■ AMBA AXI & AHB ■ Building Blocks ■ Microcontrollers ■ Foundry Libraries ■ Verification IP ■ Star IP ■ More... 	<p>Verification Suites</p> <ul style="list-style-type: none"> ■ PCI Express ■ USB OTG ■ Ethernet, SATA ■ AMBA™ 3 AXI™ ■ AMBA AHB ■ Memory Models ■ OCP ■ More... 	<p>SystemC™ Transaction-Level Models</p> <ul style="list-style-type: none"> ■ Processors ■ DesignWare Cores ■ DesignWare AMBA Components ■ Pre-Assembled Platforms



Industry's Broadest Portfolio From a Single Supplier

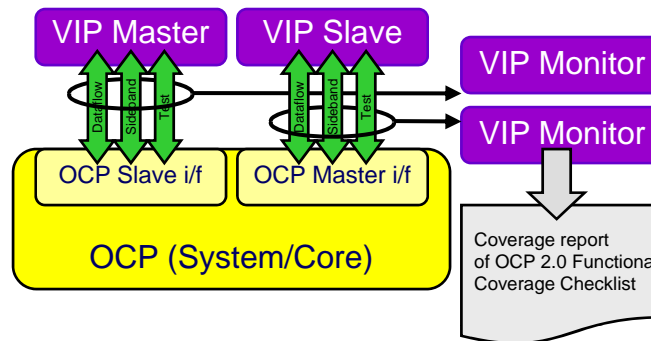
How DesignWare Verification IP improves Productivity

- Command Based Usage
 - Verilog or VHDL
 - Read, Write, Burst, etc
 - Hand-authored tests
 - Tests predicted behavior
- Object Based Usage (VMM)
 - Constrained Random Verification
 - Verification Methodology Manual
 - Functional Coverage
 - Tests predicted and unpredicted behavior



DW OCP Verification IP

Supports all OCP 2.0/2.1/2.2 dataflow & sideband transaction types



- Master initiates OCP transactions
- Slave observes the master-driven signals on the bus and initiates response procedure
- Monitor observes and reports on OCP bus activity
 - Built-In Functional Coverage of OCP-IP defined functional coverage groups
- Configuration determines which signals are in interface, how wide they are, number of concurrent transfers, timeouts, burst length, burst type etc

Supports HDL and VMM testbenches

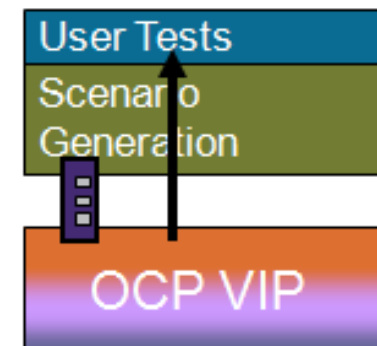
- Verilog, VHDL command interface

- Configure
- Create transactions
- Wait for callbacks
- Log transactions
- Generate coverage reports



- VMM object interface

- Constrained random configuration
- Input, output, callback channels
- Scenario Generation
- Coverage



OCP 2.2 release – January 2008

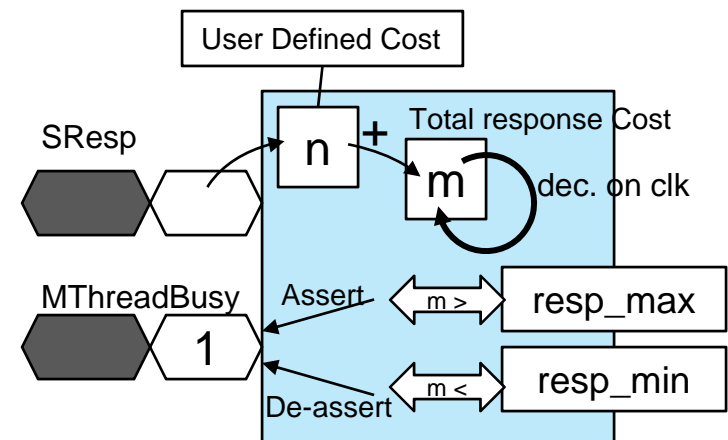
- OCP 2.2
 - Thread Busy Exact support
 - Asynchronous reset
 - Enable clock
 - 2.2 Errata
 - Block transactions (2d burst)
- Other enhancements
 - Configuration knowledgeable coverage
 - Enhanced transaction defaults
 - Alternate methods of validating threadbusy flow control

Multi-thread support

- VIP supports all Thread Busy behavior within OCP 2.2
 - Thread Busy
 - Treated as a hint by OCP-IP interfaces
 - ThreadBusy_Exact
 - Defines strict timing semantics governed by Thread Busy signal
 - Requires Thread Busy
 - Thread Busy Pipelined
 - Defines relative protocol timing affected by the Thread Busy signals
 - Requires Thread Busy Exact and Thread Busy
- VIP provides methods to model flow control
 - Provides alternative methods of validating design IP in the context of threadbusy flow control
 - Automatically drives Thread Busy signals based on selected method

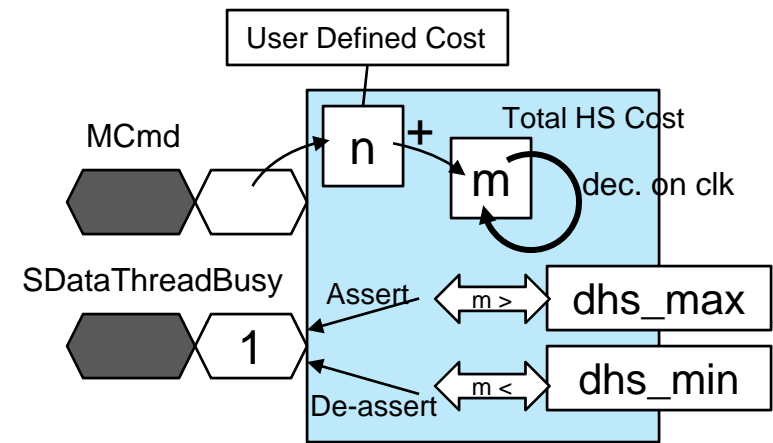
Automated MThreadBusy Signals

- FIFO method
 - Each new queued response adds a user defined response cost to the total cost for the thread
 - VIP compares total response cost to user defined req_max and req_min values
 - Asserts MThreadBusy
 - Decrements cost by one on each clock

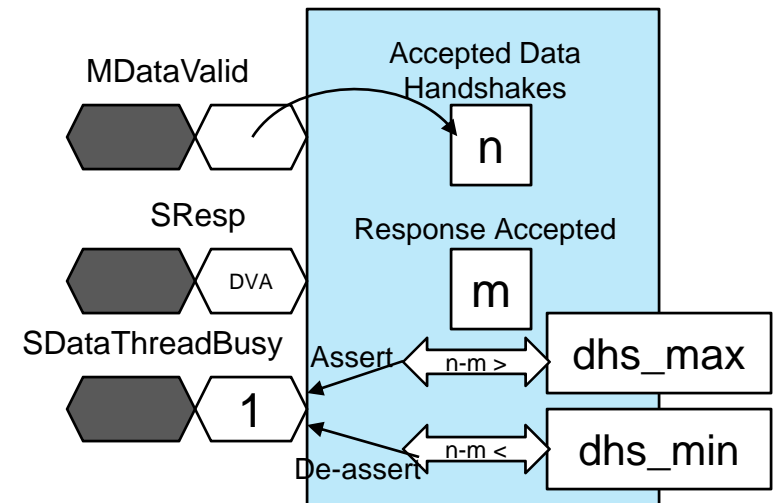


Automated SDataThreadbusy Signals

- FIFO Method
 - Each new request adds a user defined handshake cost to the total cost for the thread
 - VIP compares total cost to user defined dhs_max and dhs_min values
 - Asserts SDataThreadBusy
 - Decrements cost by one on each clock



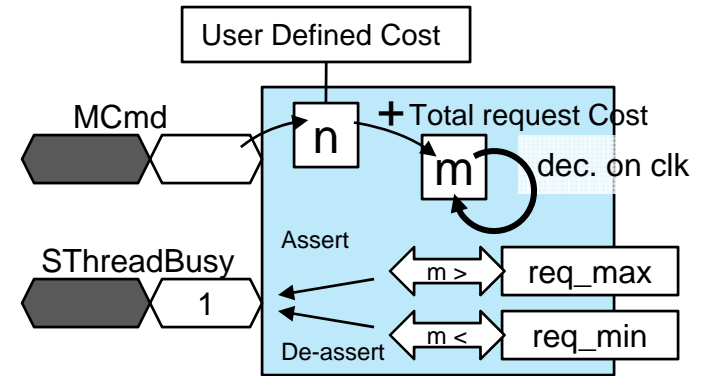
- Response Method
 - VIP monitors accepted response pipeline and data handshake pipeline
 - Depends on write transactions that require responses
 - Calculates the difference between datahandshake queue and response queue, and compares to dhs_max and dhs_min
 - Asserts SDataThreadBusy



Automated SThreadbusy Signals

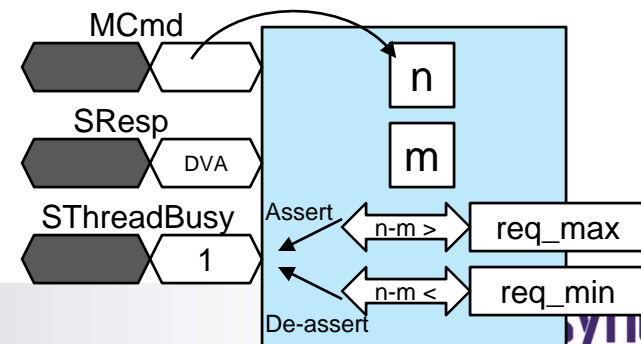
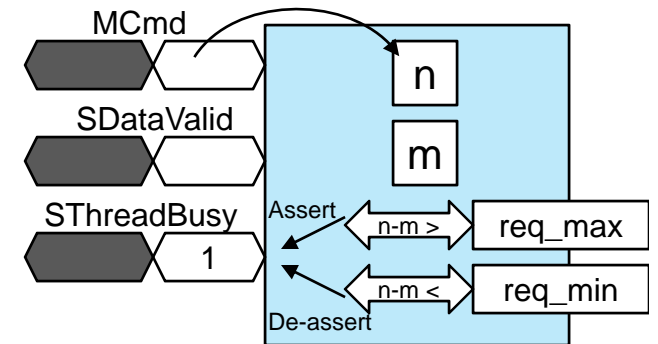
- FIFO method

- Each new request adds a user defined request cost to the total cost for the thread
- VIP compares total req cost to user defined req_max and req_min values
 - Asserts SThreadBusy
- Decrements cost by one on each clock



- Outstanding DataHandshake / Response Methods

- Data (Write Transactions Only, using Data Handshake Pipeline)
 - VIP monitors difference between the number of accepted requests (n) and completed handshakes (m), and compares to req_max / req_min values
- Response (using response Pipeline)
 - VIP monitors the difference between the number of accepted requests (n) and number of responses accepted (m) and compares to req_max and req_min values
- Asserts SThreadBusy



DesignWare Verification IP Benefits

- **Saves testbench development time**
 - Easy to integrate into your current methodology
 - Provides coverage reports and protocol checks
- **Reduces project risk**
 - Enables verification of full breadth of each protocol
 - Support for constrained random verification
 - Tests for corner cases behavior
- **Highest quality**
 - Design proven on hundreds of customer designs
 - Extensive regression environments
- **Part of the industry leading verification IP portfolio**
 - Broadest collection of verification IP titles

