



T H E C O M P L E T E S O C K E T

OCP Debug Socket for Multi-Core Debugging

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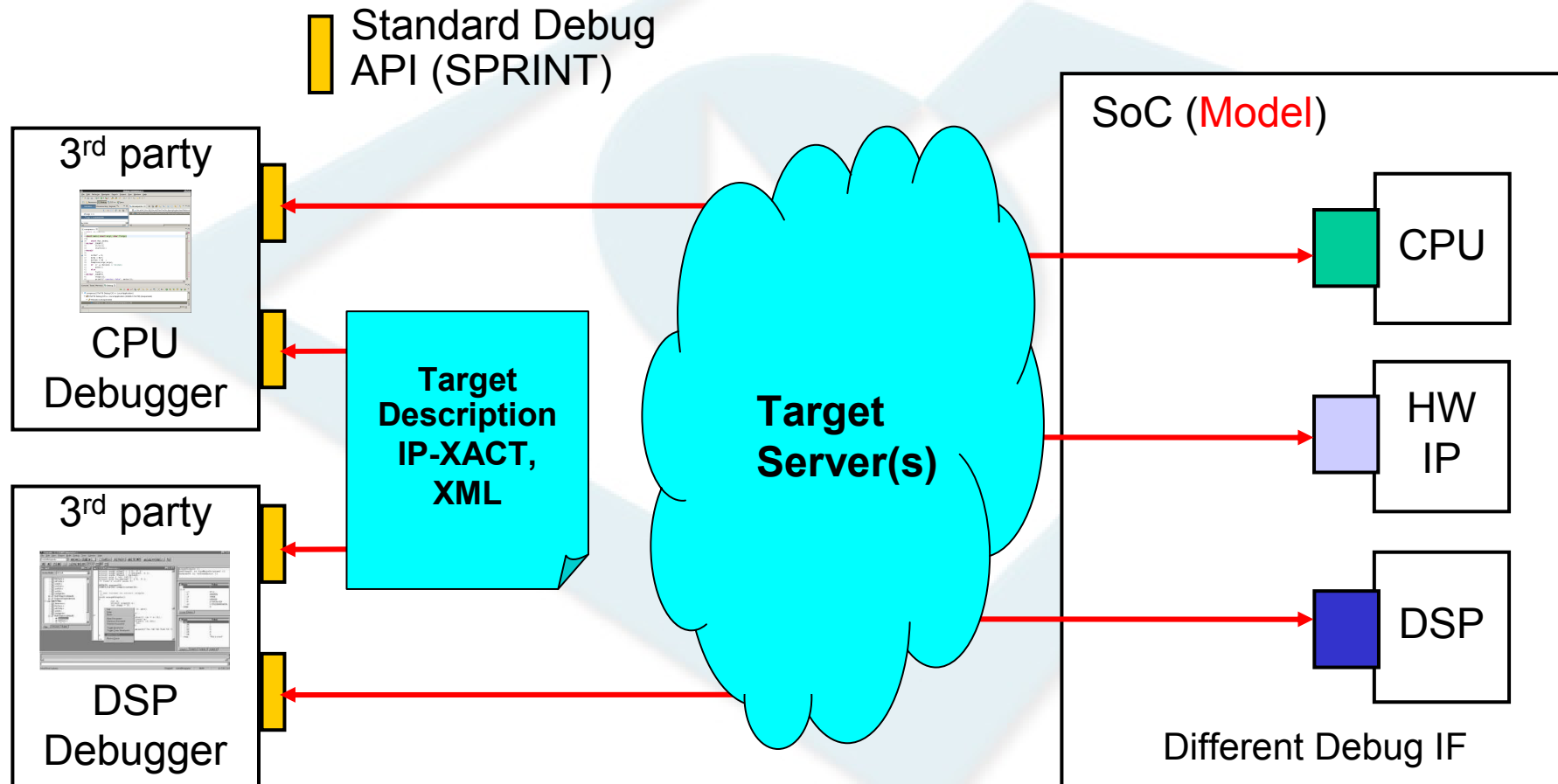
OCP-IP announces the release of its Debug Standard.

The new standard identifies Basic and Extended sets of socket level signals for debugging of multiple processor cores connected with the OCP interface.

The standard represents a breakthrough allowing designers to distribute debug signals as part of the system interface scheme; rather than wired separately from the data path as had been previously been the case.

This innovative new approach greatly enhances system providers ability to prepare multi-core debug hardware and software.

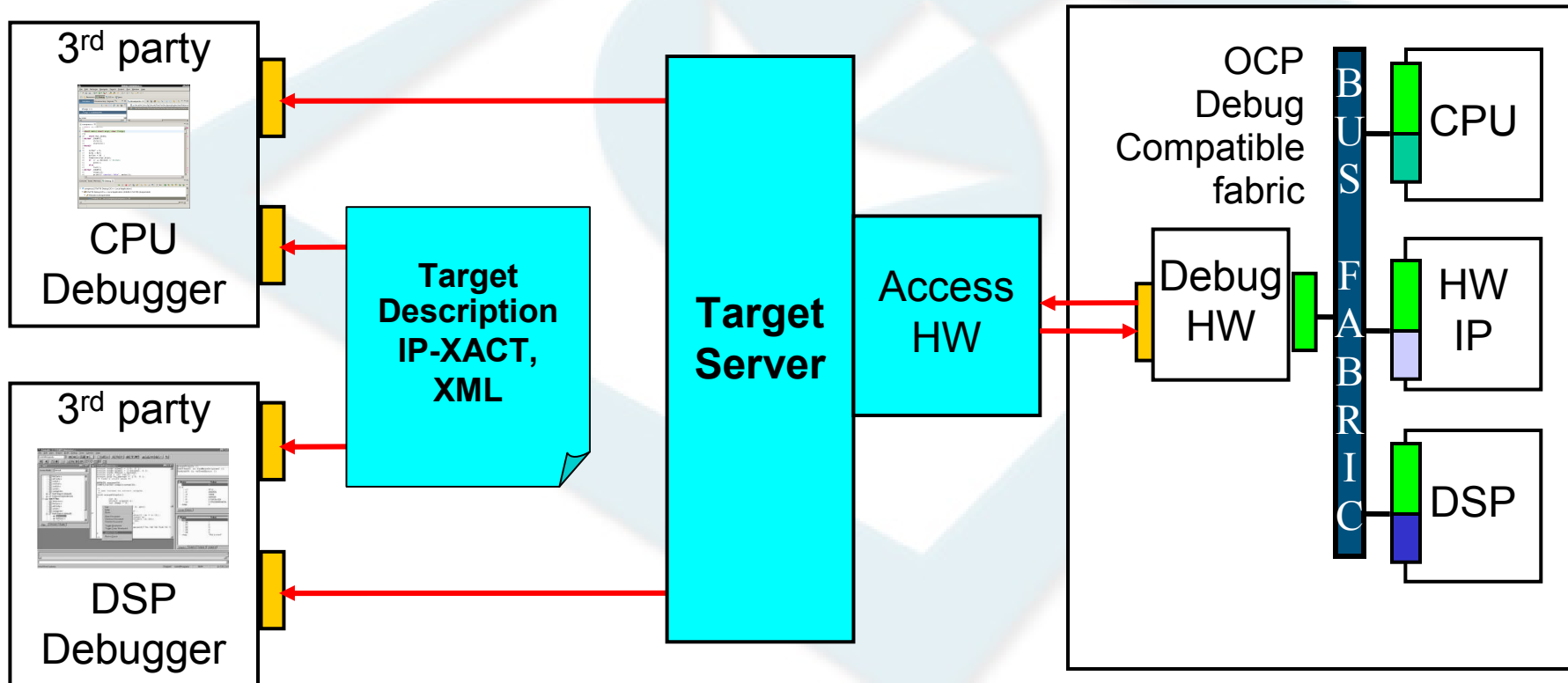
Debug Environment



NEW OCP Debug Standard

Standard Debug API (SPRINT)
 Basic OCP Debug Interface

 Extended OCP Debug Interfaces



The SPRINT software standard is related to our work as a general debug functionality description for multiple processors.

OCP Debug Standard Advantages

Simplifies debug - Standardized Basic OCP Debug Socket for all OCP IP

- Several application specific options

Debug Hardware and Software for multi-core debugging can be offered as standard IP

Opens implementation and support of more (heterogeneous) processors inside one debug GUI

Proprietary Debug solutions supported - Need just OCP Debug wrapper

Fixed OCP debug interface, is still open to a multitude of debug interconnects (I.e. Nexus style, or serial buses, or cross bar, or NoC, etc)

We expect high uptake of the new standard in the OCP-IP community (Reusable IP blocks)

Connection with SPRINT

SPRINT's functionality API is utilized for multiple core debugging.

The SPRINT Debug API is related to the OCP-IP standard as a general debug functionality description for multiple processors.

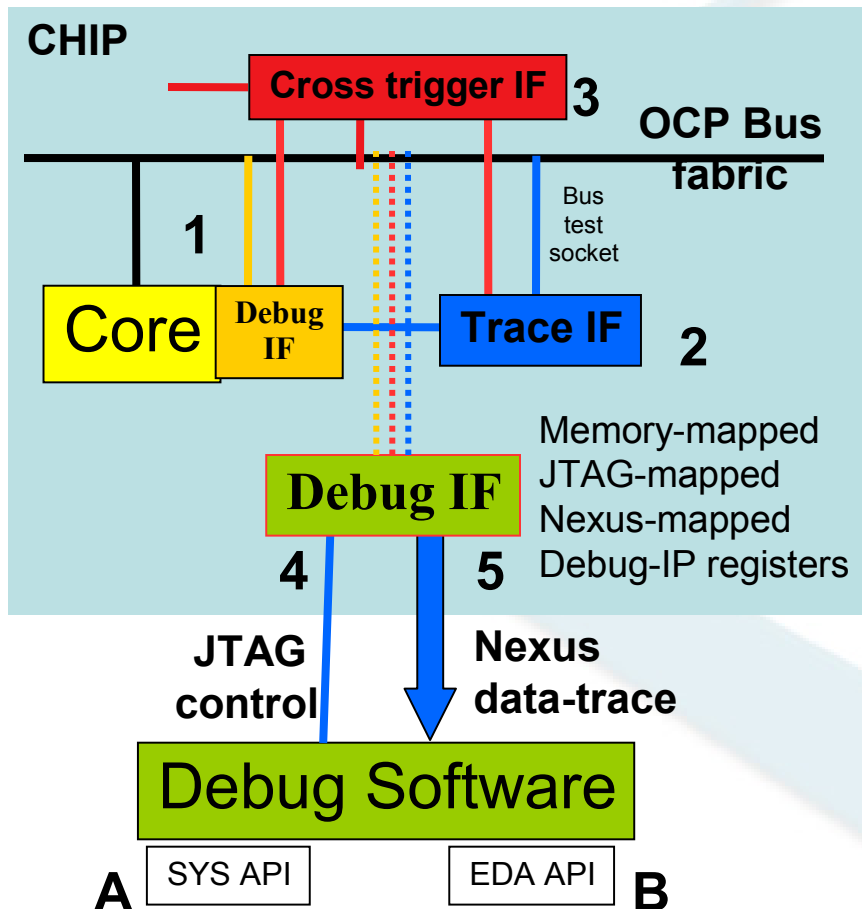
SPRINT's Debug API defines all the transactions and formats that must be realized by the debug hardware and is supported by the OCP-IP standard.

SPRINT is providing the definition of the debug functionality which we refer to in the OCP-IP Debug standard.

The SPRINT Debug API is expected to be available on GreenSocs.com Q208.

Definition of Debug Hardware-IP Block and Environment

SoC Debug Solutions Have 5 Hardware and 2 Software Interfaces



Debug-IP HW connections to SoC:

1 CORE-INTERFACE: interfaces to core IP-block debug data/control proprietary IO

2 BUS-INTERFACE: interface to a bus traffic [event/trace data collect, compression and triggering]

3 CROSS-TRIGGER INTERFACE: to other debug-IP blocks [event-synch.]

4 PIN-INTERFACE CONTROL: IF to JTAG for debug control to analyser/debugger software.

5 PIN-INTERFACE DATA: interface for high speed data [like Nexus]

Debug software API for information transfer and display:

A. System Debug SW API interface

B. EDA API interface – block and system level verification (ESL, RTL)

Essential Debug Infrastructure

Standardized OCP Debug solution consists of:

- Debug hardware for multi-core OCP Debug Sockets
- Debug software for 2 or more cores in one GUI (following SPRINT recommendation)
- XML file to expose debug topology and processor cores (following SPRINT rules)
- XML file to define the OCP Debug Interface signals (following SPIRIT framework)
- OCP interconnect generator to automate debug sockets wiring on a chip

The central OCP-IP Debug Standard mission is to define the first two.

The next three substantially increase comfort when working with debug solutions.

What is in the Debug Specification?

OCP Interface for Basic Debug Signals

- **Debug Control and Run Control for Cores**
 - **Consistent (multiple) processor software debugger interfaces**
- **Cross-Triggering between Multiple Cores and Events**
 - **Scalable to on-chip/off-chip cross triggering**
- **Trace Interface**
 - **Bus traffic observation (system trace) and control (triggering)**
- **New classes of debug errors (different from system errors)**

OCP Interface for Extended Signals (Special features)

- **Performance Monitor**
- **Time-stamping**
- **Power Monitoring voltage islands, gated clock islands**
- **Security islands**

Of huge value
in final silicon

OCP Debug Interface Signals, BASIC

Reset Socket

Debug_rest_n
Debug_en

JTAG Socket

Tck
Trst
Tms
Tdi
Tdo

Control Socket

ReqDebug
Msuspend
DebugSerror
DebugCon
NoSResp
ForceResp
ForceAbort
ForceAbortAck

Trace Socket

TraceTrigger[x]

Triggering Socket

Trigger_in_condition[n:0]
Trigger_out_action[n:0]
Trigger_out_enable[n:0]
Ext_trig_clk
Ext_condition[n:0]
Ext_action[n:0]

Run Control Socket

SyncRun
SyncRunAck

OCP Debug Interface Signals, EXTENDED

Performance Monitoring Socket

MConnID

MchannelID

MreqWatch[x]

PMSampling

Timestamp Socket

Ts_clk

Ts_reset

Power Monitoring Socket

Srbbsp[2:0]

PWRDomainStatus

CLKDomainStatus

Security Socket

MreqSecure

DebugMode[1:0]

TraceMode[1:0]

TAPenable

Summary

Main philosophy is:

Debug N cores on a chip by selecting any 2 or more cores for a time-aligned comparative debug session.

OCP-IP has standardized the Debug Interface between system bus and any/multiple processor cores and IP-blocks in a SoC design.

- **Enables reusable multi-core Debug-Hardware solutions. (OCP/JTAG/Nexus/MIPI)**
- **Enables Debug-Software for multiple cores in one GUI. (See SPRINT debug APIs)**
- **This will open the market for SoC designers to buy verified multi-core debug-IP solutions. (See IP-Extreme, HDL-Dynamics, Temento, ... IP providers)**

OCP Debug Information

- OCP public white papers are at: www.ocpip.org/socket/whitepapers/
- OCP members get the standard at: www.ocpip.org/members/ocpspec/
- OCP membership admin: admin@ocpip.org
- Non-members can access this standard using an on-line, click-through research License
- **Visit the OCP booth *F42* at DATE 2008!**